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Current Status and outlook for EUV mask

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Outline

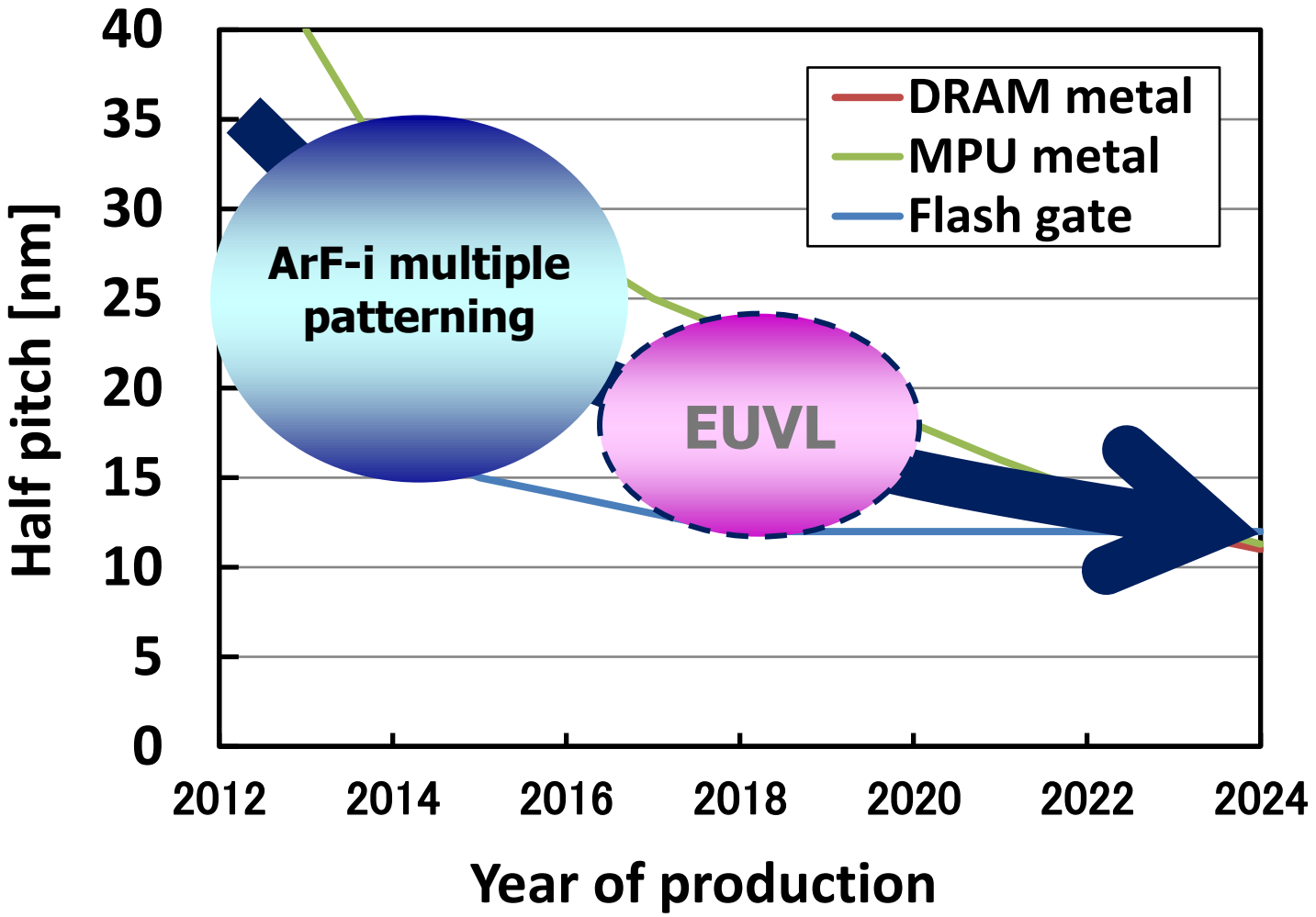
[1] Introduction

[2] Defect Management
- (1) EUV Blank/Mask Infrastructure
- (2) Defect Management for HVM

[3] EUVL Extension
- (1) Challenges for EUVL Caused by 3D Mask Effect
- (2) Etched ML Mask

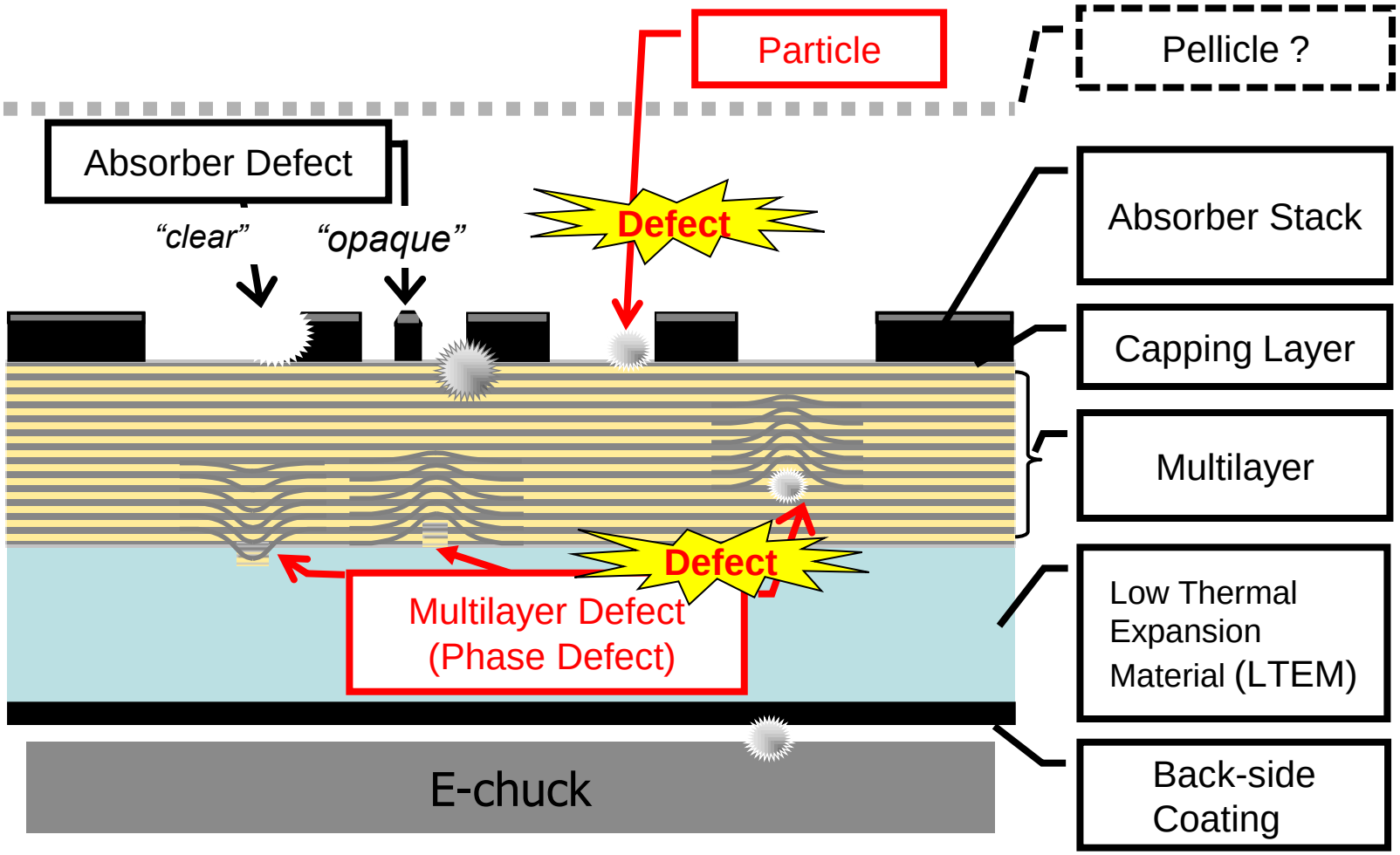
[4] Summary

Scaling Road Map



Ref: ITRS 2013 Edition

Current EUV Mask Structure and Challenges



Mask yield & defect inspection/review infrastructure is key challenges for HVM insertion.

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Blank/Mask Defect Inspection Infrastructure

Commercially available

hp16nm HVM and beyond

Blank Inspection (BI)

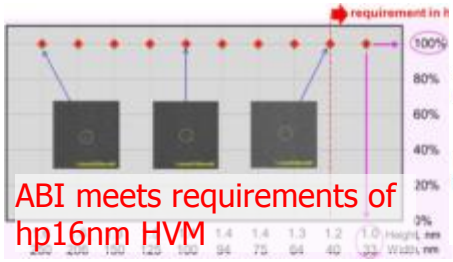
✓ MAGICS (Lasertec)

266nm/
355nm/ 532nm
wavelength

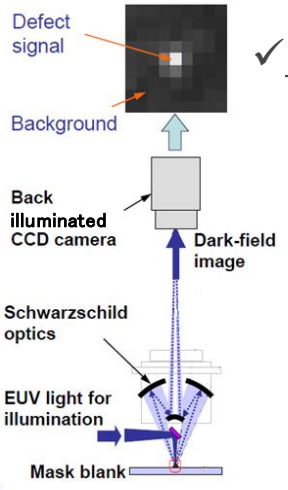
http://www.lasertec.co.jp/

✓ Actinic BI (EIDEC/Lasertec)

H. Watanabe, EUVL symposium 2013



ABI meets requirements of hp16nm HVM



Pattern Inspection (PI)

✓ Teron6xx(KLA-T)

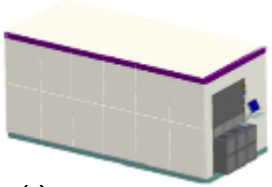
193nm wavelength

http://www.kla-tencor.com/

✓ KLA 7xx(KLA-T)

T. Yamamoto, EUVL symposium 2013

Actinic Pattern/Blank Inspection



✓ NPI-7000 (Nuflare)

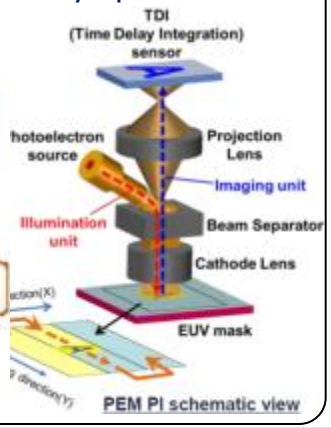
199nm
wavelength

http://www.nuflare.co.jp/

✓ EB PI (EIDEC/EBARA)

PEM (Projection Electron Microscope) technique

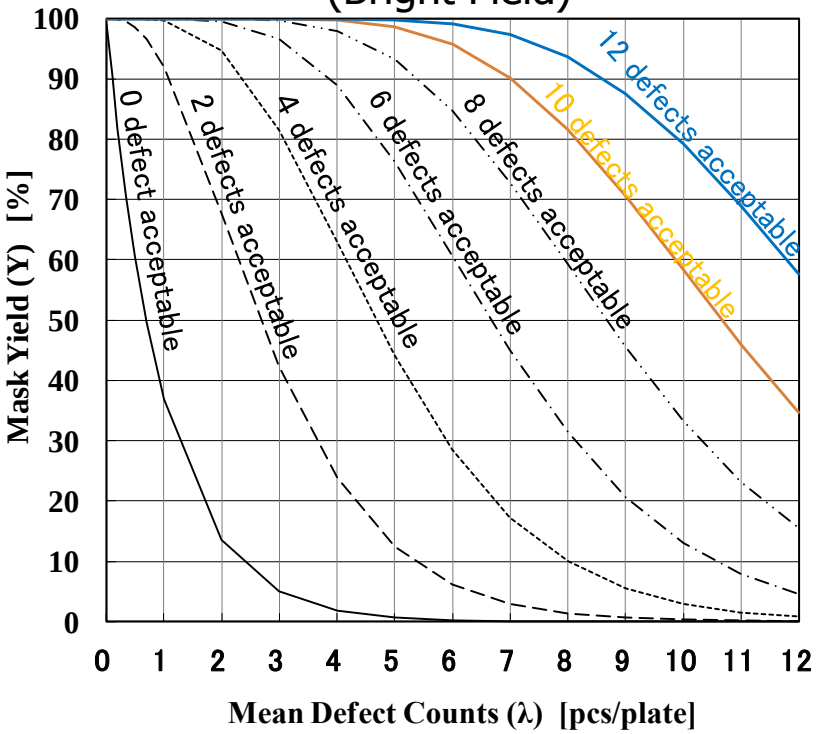
R. Hirano, EUVL symposium 2013



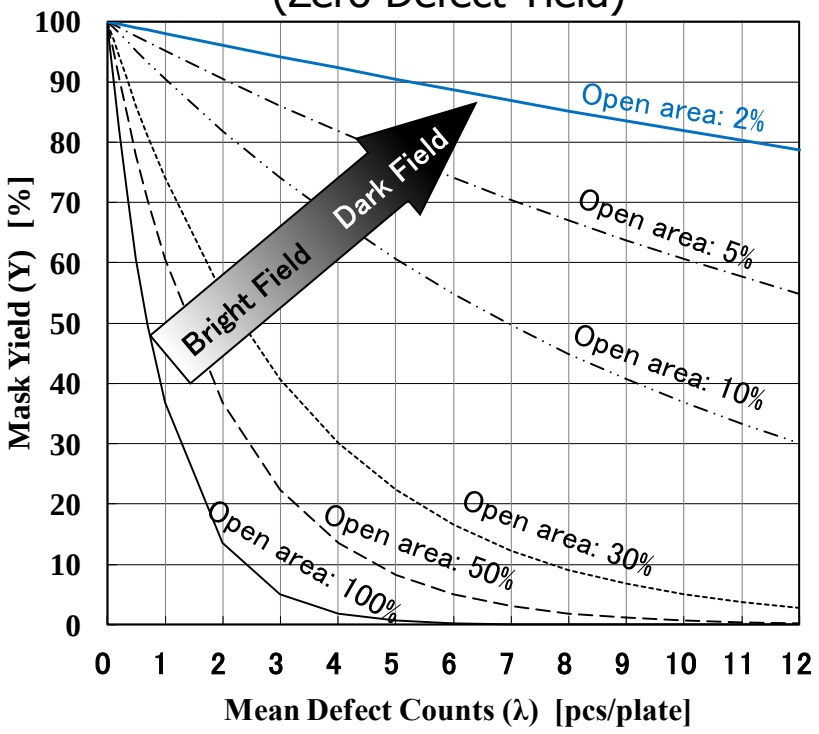
Mask Defect Yield vs Defect Counts

Estimation from Poisson Distribution

Dependency on acceptable defect counts (Bright Field)



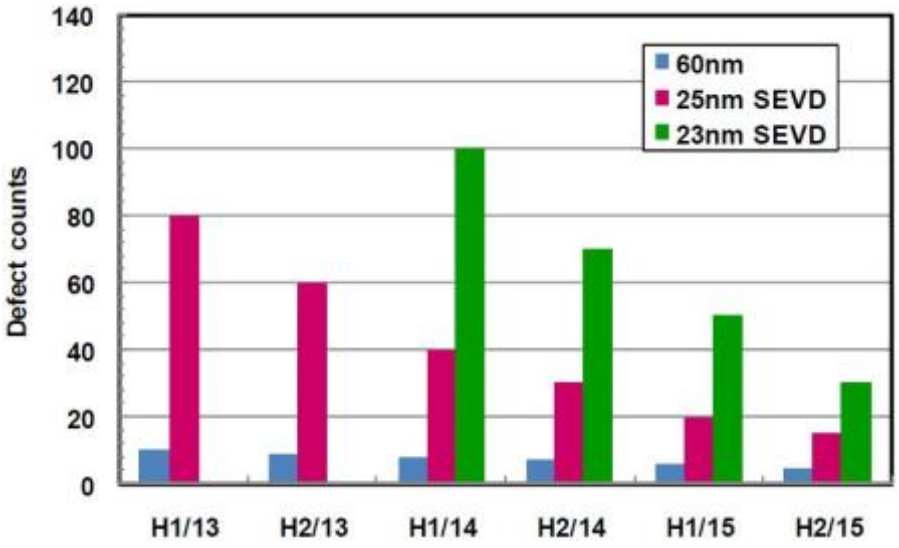
Dependency on pattern variation (Zero Defect Yield)



	Mean defect counts	Estimated yield of mask defect (Bright Field)
Pilot	0.5	60%, 99.99% (if 4 defects are accepted)
HVM	0.001	99.9%
HVM	0.0001	99.99%

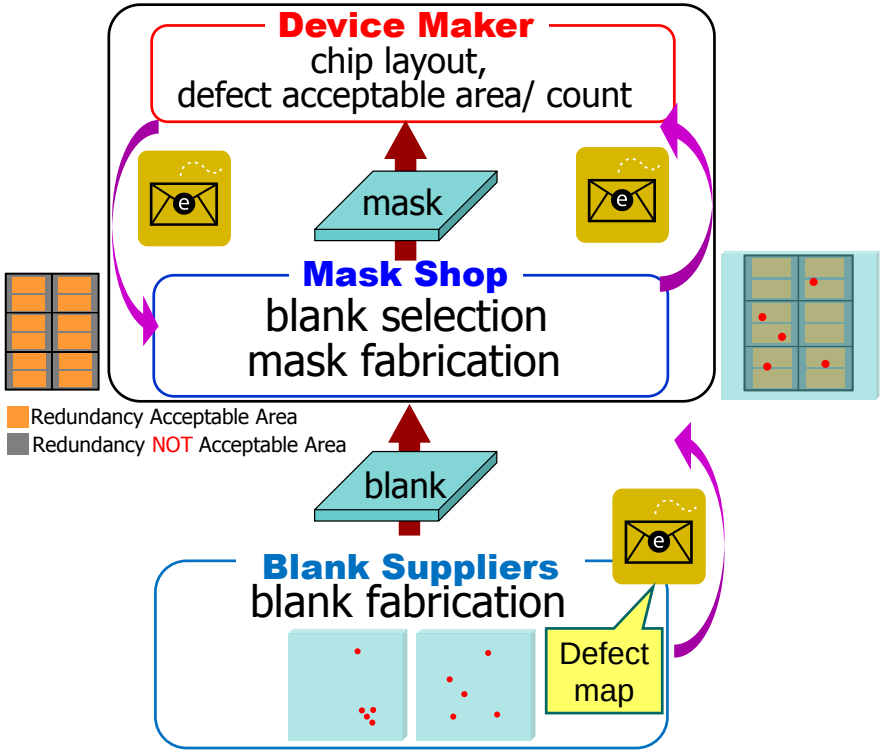
Blank Defect Roadmap and Blank Supply Chain

ML Blank Defect Roadmap by Blank Supplier



by courtesy of HOYA

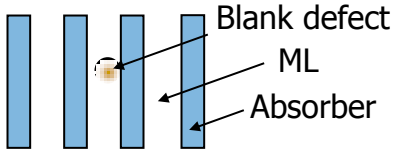
Blank Supply Chain



Supply chain management with blank supplier is necessary.

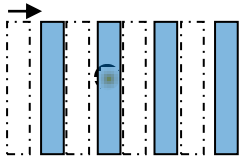
Blank Defect Mitigation by Pattern Shift

Method of Blank Defect Mitigation



Impact on wafer printability will be reduced by

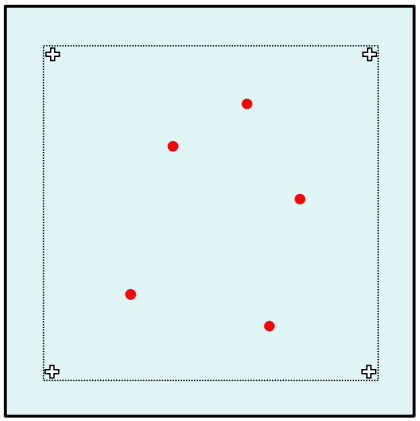
Pattern shift



covering blank defect with absorber

Position Accuracy in Blank Defect Mitigation with Pattern Shift

Blank Defect Map with FM

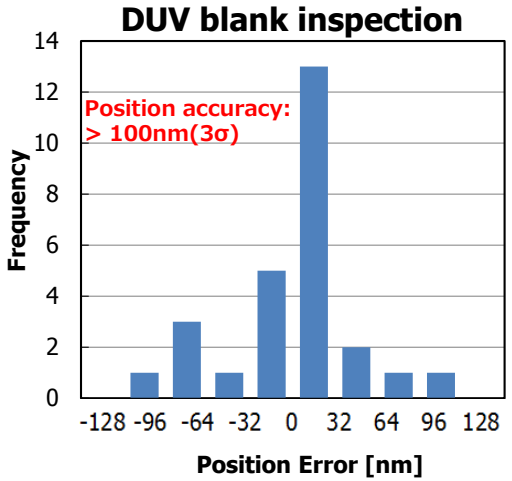


Position Accuracy Requirement of Blank Defect

	40nm Defect	24nm Defect
hp64nm L/S (4x)	+/- 12nm	+/- 20nm

Target: 20nm(3σ)

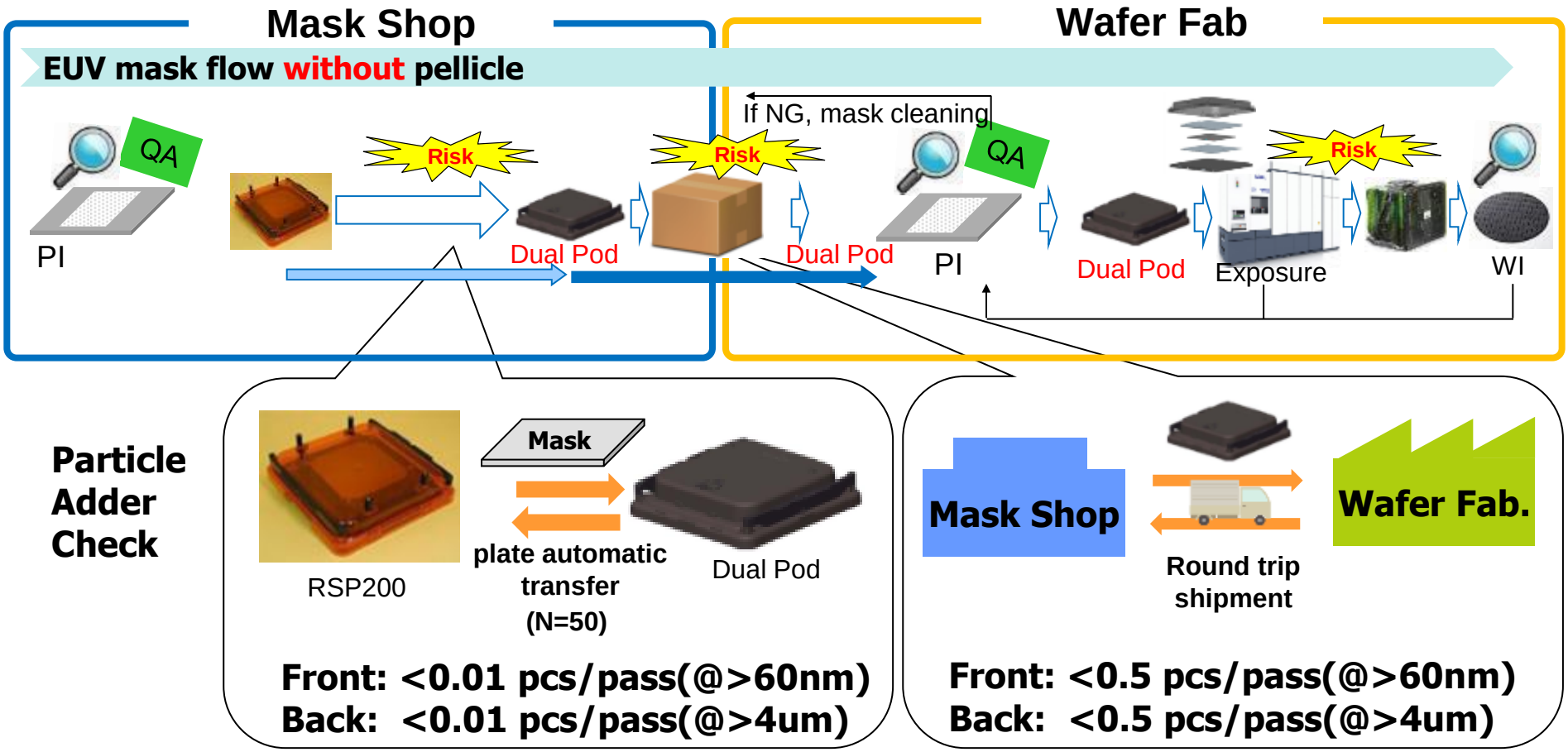
Blank Defect Position error



Origin of position error: Position accuracy（BI, EB writer）, Alignment error including FM reading

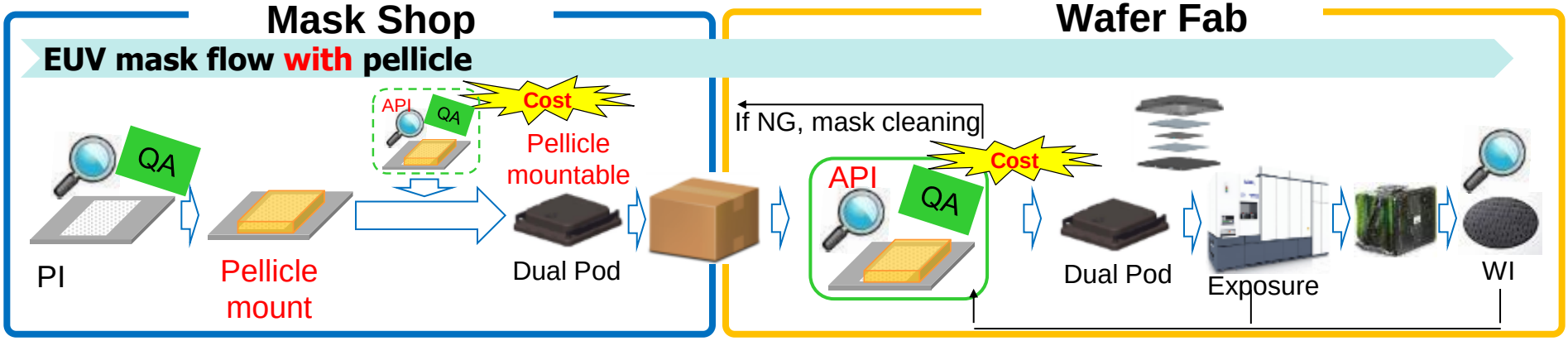
Current blank defect position error of DUV BI is >100nm. Blank defect position error is to be reduced to within 20nm (3σ) with ABI tool.

EUV Mask Defect QA Flow and Challenges

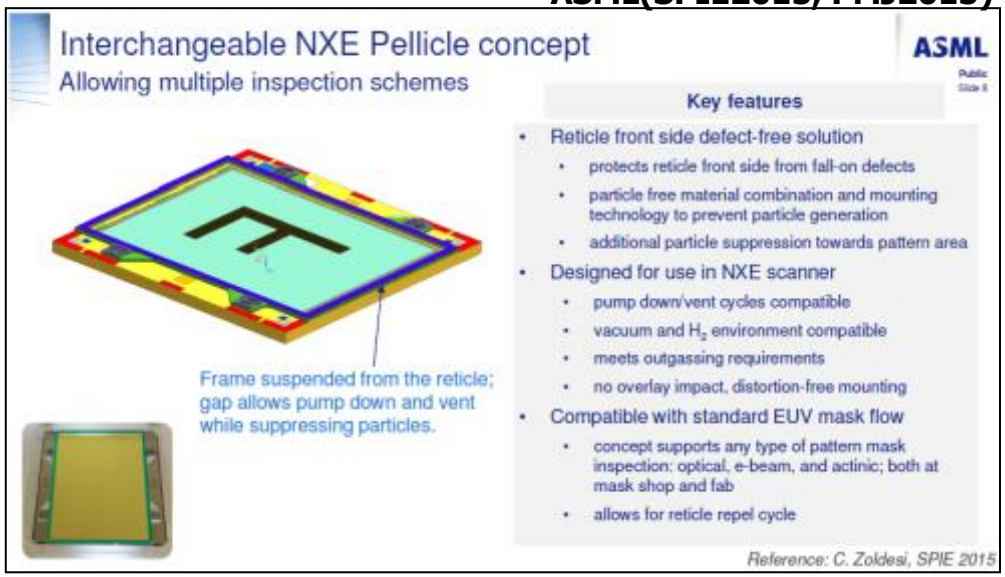


EUV mask handling with dual pod shows encouraging results for the devices in which redundancy is applicable.

EUV Mask Defect QA Flow and Challenges



ASML(SPIE2015, PMJ2015)



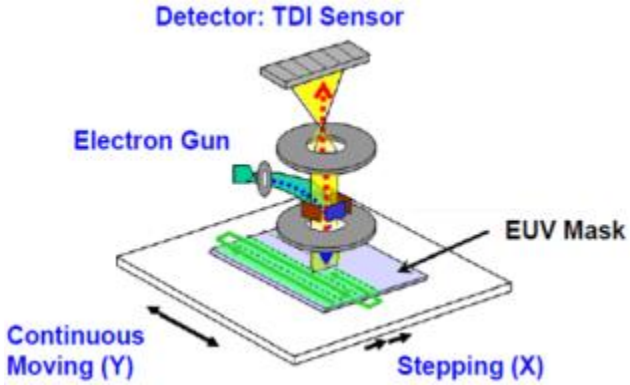
Interchangeable pellicle concept is proposed by ASML to meet multiple inspection schemes (DUV, EB, API).

Severe particle management is still necessary for EUV mask with pellicle because EUV pellicle proposed by ASML has a gap between mask pattern surface and pellicle frame.

New EUV pellicle system attachable only in exposure tool is preferable from the mask fabrication viewpoint.

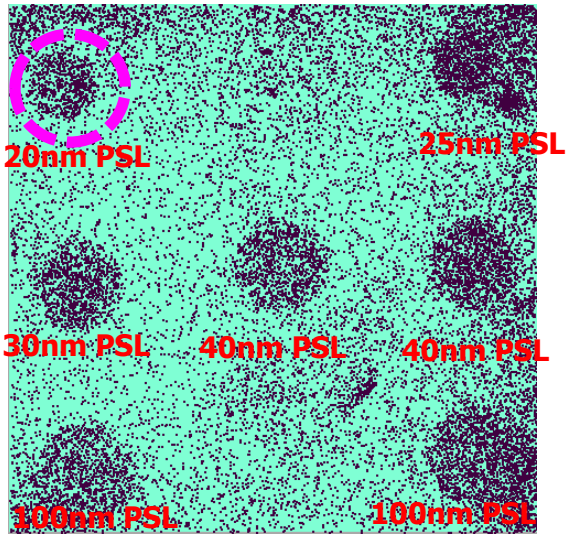
EB Inspection for Particle Monitor

Model EBEYE M (EBARA)

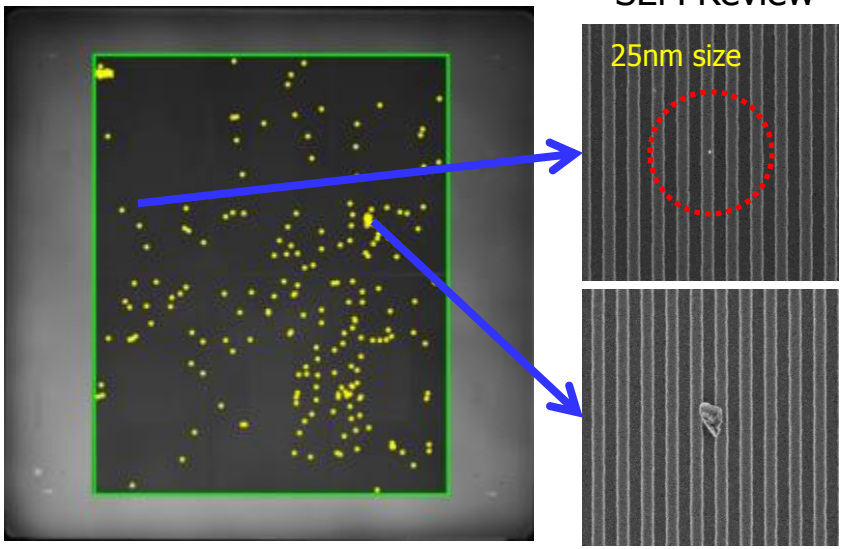


PEM (Projection Electron Microscope) can detect 20nm PSL with high throughput (1H@100mmx100mm□).

PSL dispended blank



Patterned EUV mask



EBeyeM is to be used for particle inspection in EUV mask handling.

EUV Mask Infrastructure Readiness

	hp2xnm	hp1xnm	
Multilayer Blank Inspection	DUV	Actinic	
Pattern Inspection	DUV	EB	Actinic
Particle Inspection	DUV/EB	EB	
Defect Repair	EB Repair	EB Repair	
Mask Defect QA	SEM + Litho. Simulation	SEM + Litho. Simulation	AIMS-EUV

ready

under developing

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- **(1) Challenges for EUVL Caused by 3D Mask Effect**
- **(2) Etched ML Mask**

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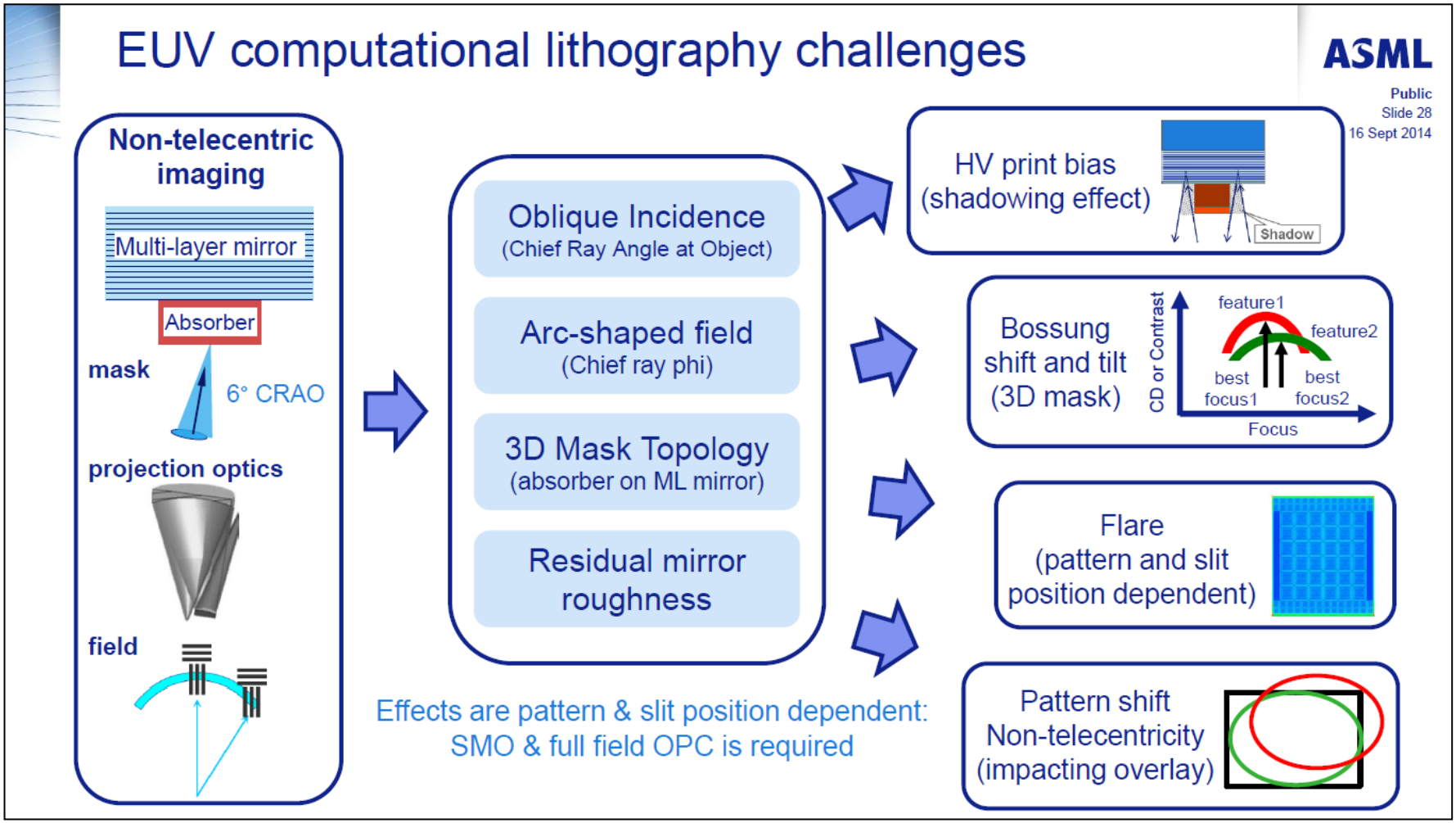
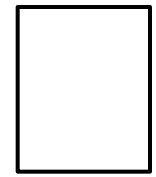
Challenges for 0.33NA EUVL Caused by 3D Mask Topology

ASML(BACUS2014)



As target pattern shrinks, the hurdles induced by mask 3D topology go higher in 0.33NA EUVL system.

Challenges for High-NA EUVL and Solution



X Mag. = (6 or 8)

9/12inch Mask

FF(26x33)

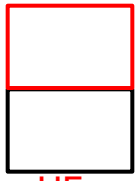
- Infrastructure for large mask

Resolution

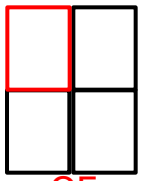
High-NA EUVL trade off

Full-field

6inch mask



or



X Mag. = (5 or 8)

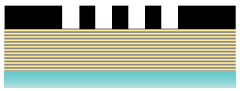
6inch Mask

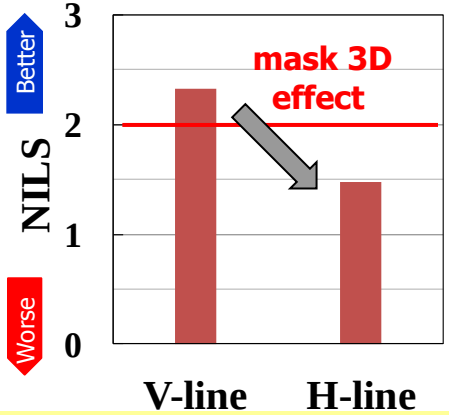
HF (16.5x26)

QF (13x16.5)

- Low exposure throughput
- Stitching technology

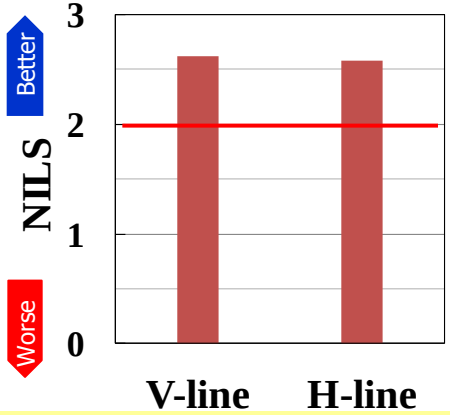
Ta based absorber





lower mask 3D effect

Etched Multilayer



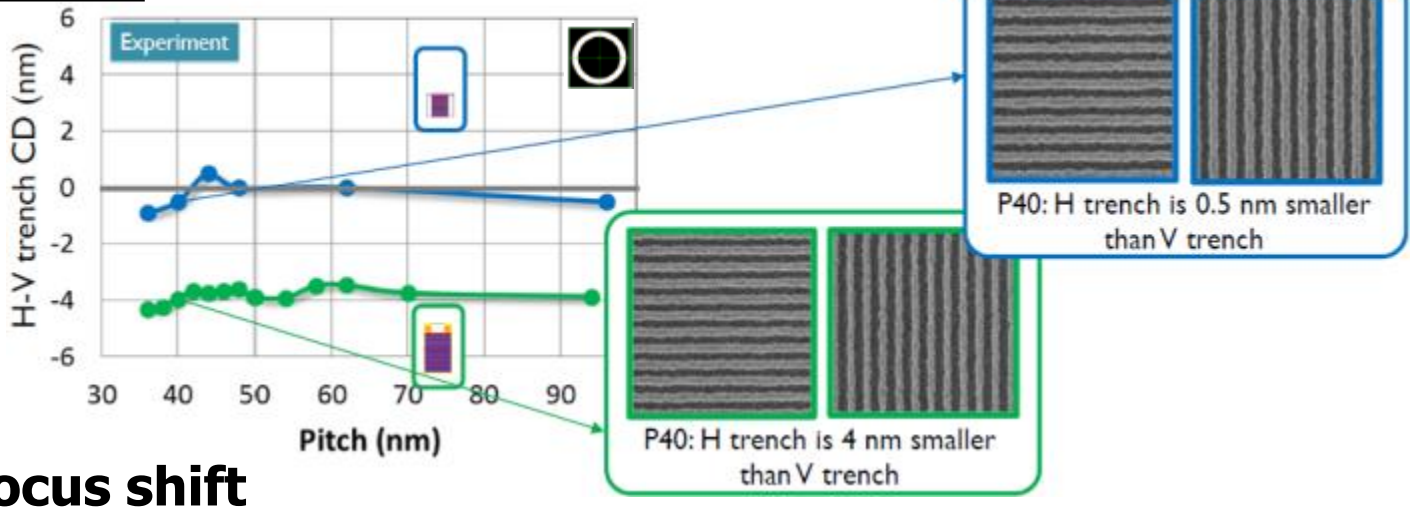
NA=0.5, CRA=8deg hp10nm

Etched multilayer mask can solve high-NA EUVL trade off (full-field, 6inch mask, high wafer resolution).

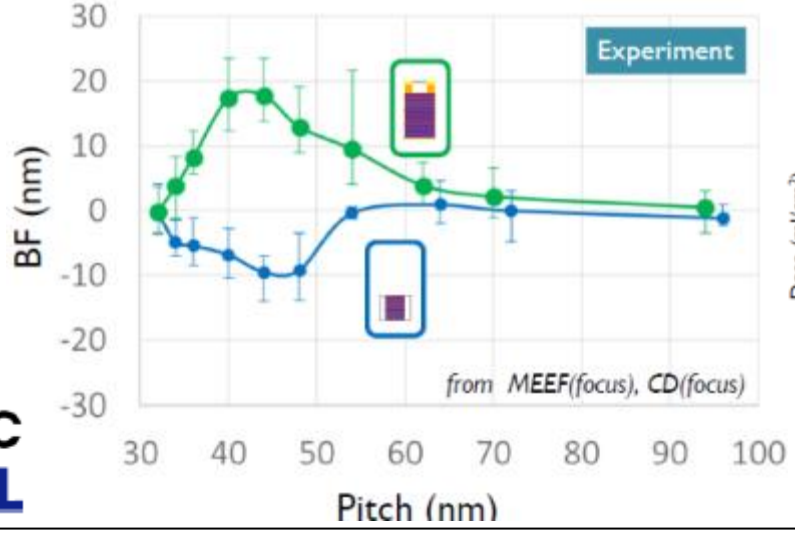
NXE3300 Exposure Result (Etched ML Mask vs Conv. Mask)

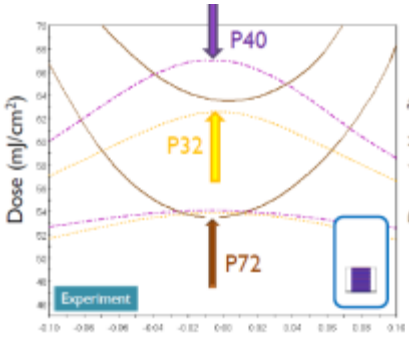
imec/ASML/Zeiss (PMJ2015)

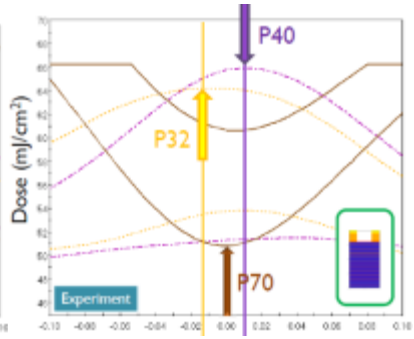
H-V CD bias



Best focus shift





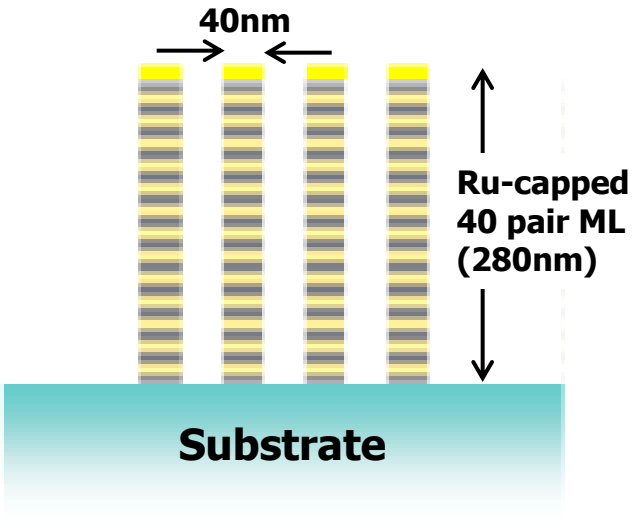


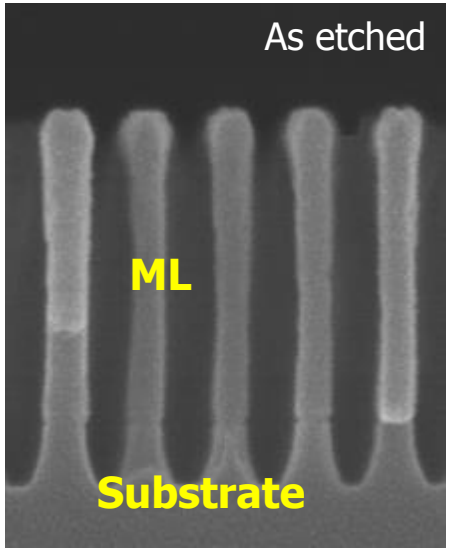
imec
ASML

Lower mask 3D effects of etched ML mask has been demonstrated in 0.33NA exposure system.

Challenges for Etched Multilayer Mask

Illustration and X-SEM image of **etched ML mask pattern of hp 40nm** (corresponds to hp10nm on wafer)

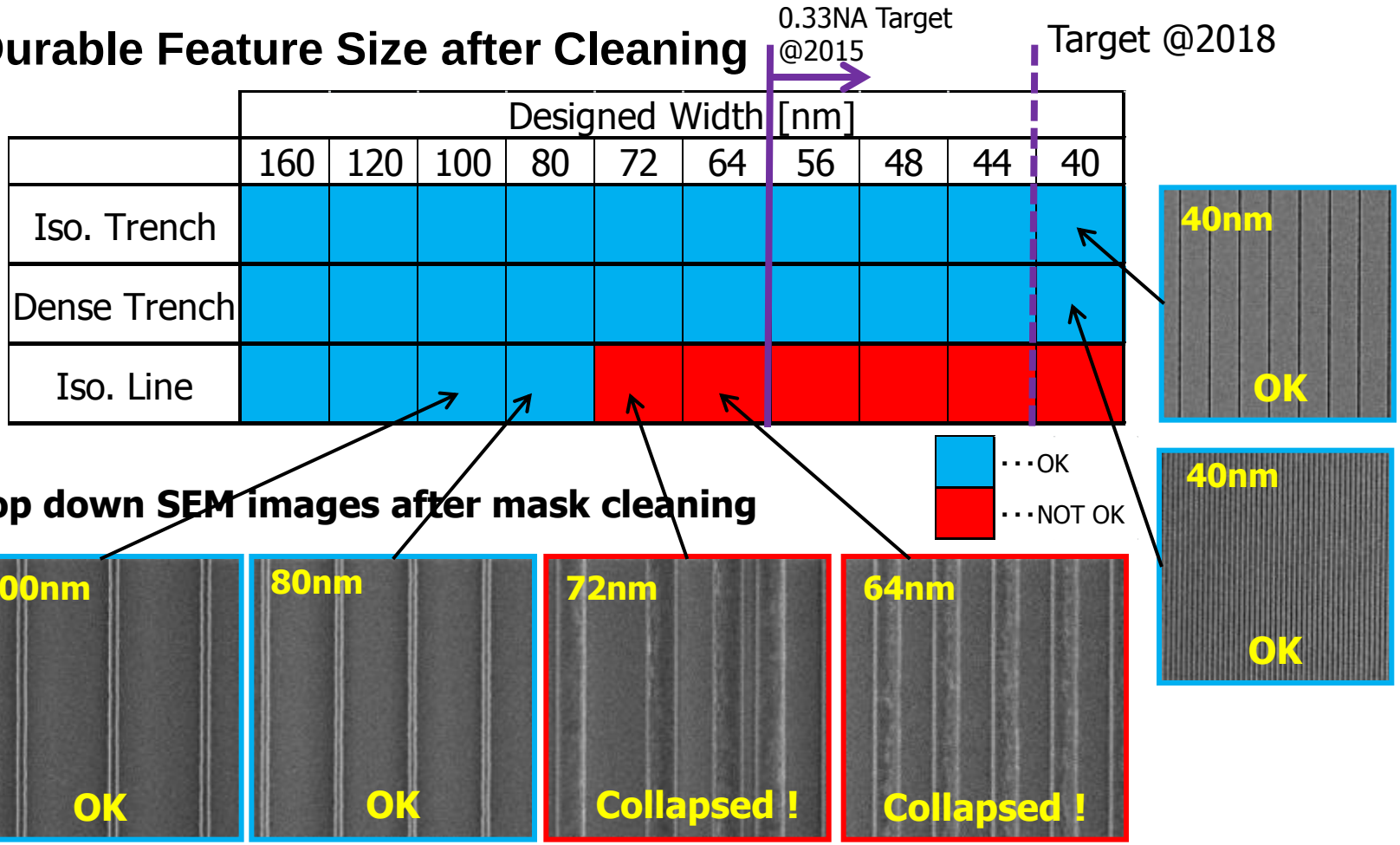




- Mask CD/ profile control
- ML pattern collapse durability against mask cleaning
- Defect inspection
- Repair of ML pattern intrusion defect
- .....

Cleaning Durability of Etched ML Pattern

Durable Feature Size after Cleaning

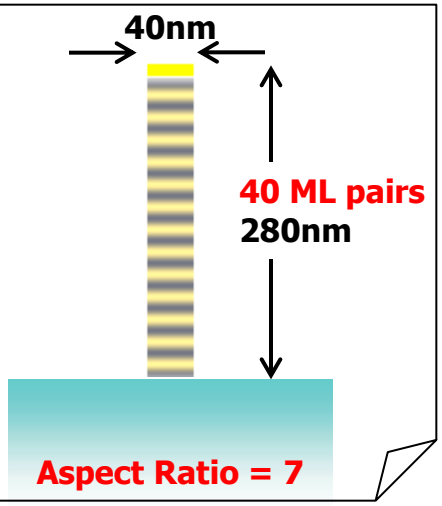


Isolated/dense 40nm trench pattern is obtained, however, isolated 72nm line is collapsed due to low cleaning durability.

Root Cause of Pattern Collapse and Solution

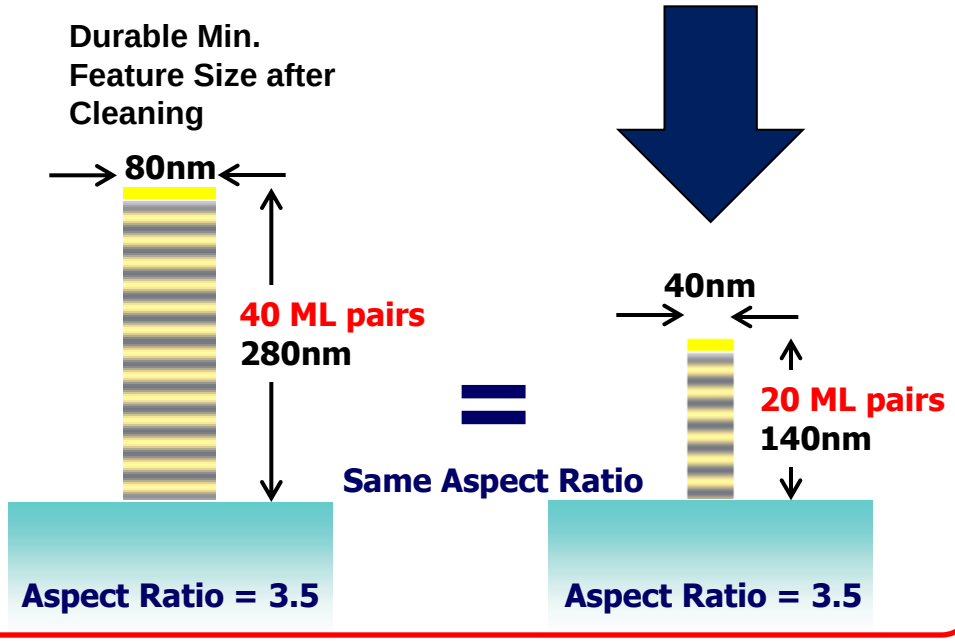
Root Cause of ML Pattern Collapse:

- Large bending force **caused by high aspect ratio** of ML pattern during mask cleaning



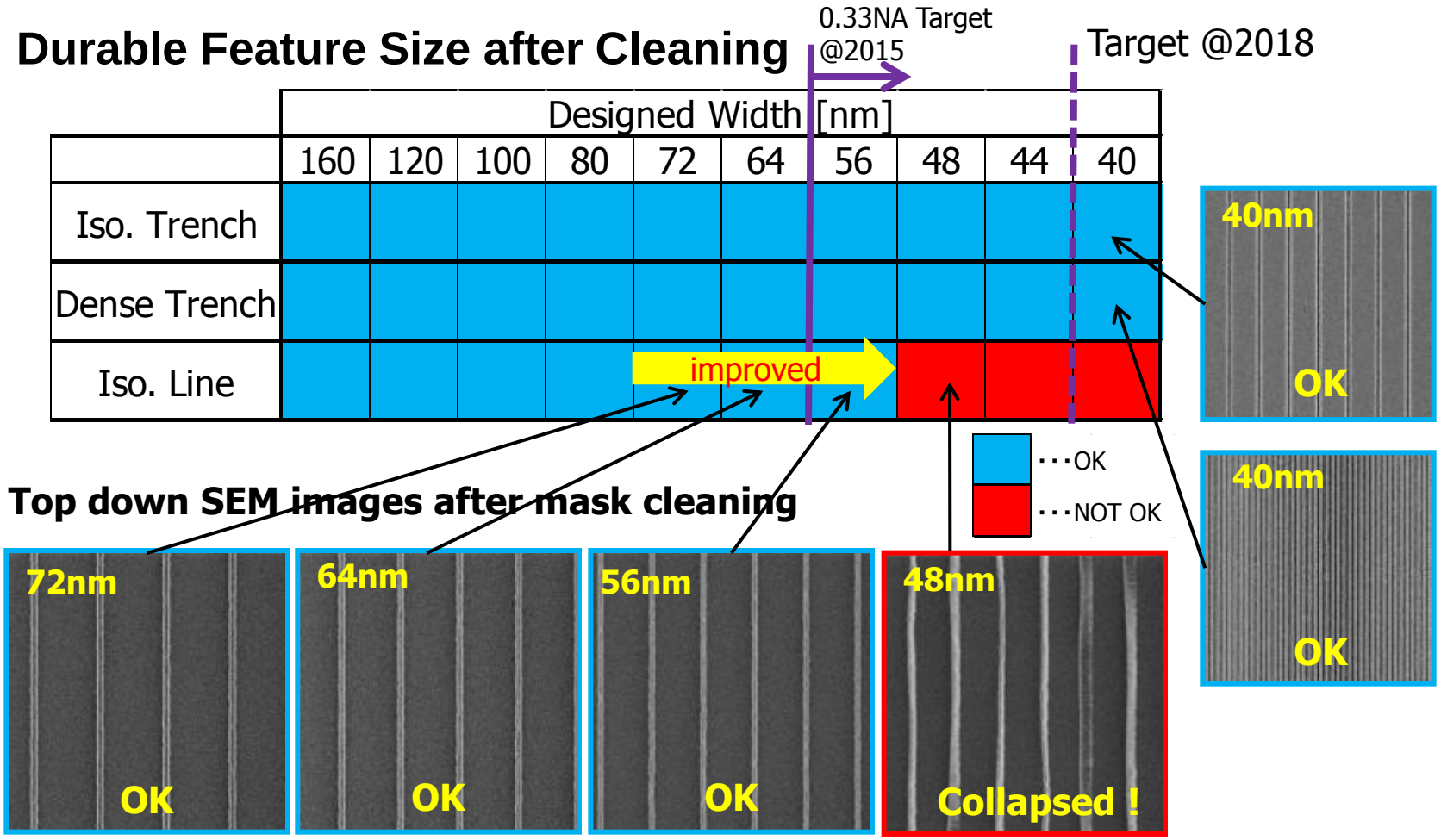
Solution:

- **Reducing 40 ML pairs to 20 ML pairs** which correspond to the same aspect ratio of durable mask topology



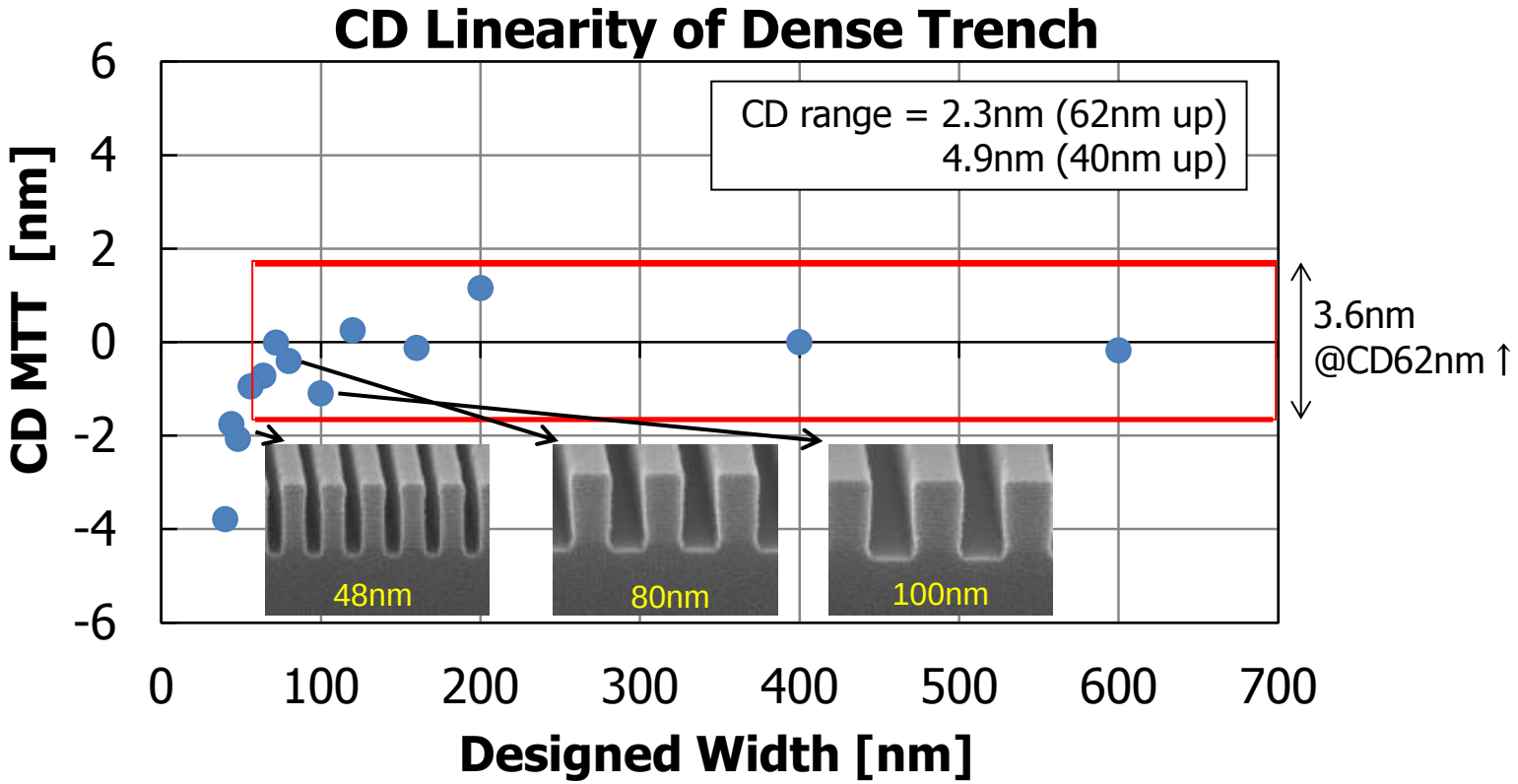
Cleaning Durability of Etched 20ML Pattern

Durable Feature Size after Cleaning



Durable minimum size is improved to 56nm at isolated line.
0.33NA CD target @2015 is achieved by simply reducing ML pairs.

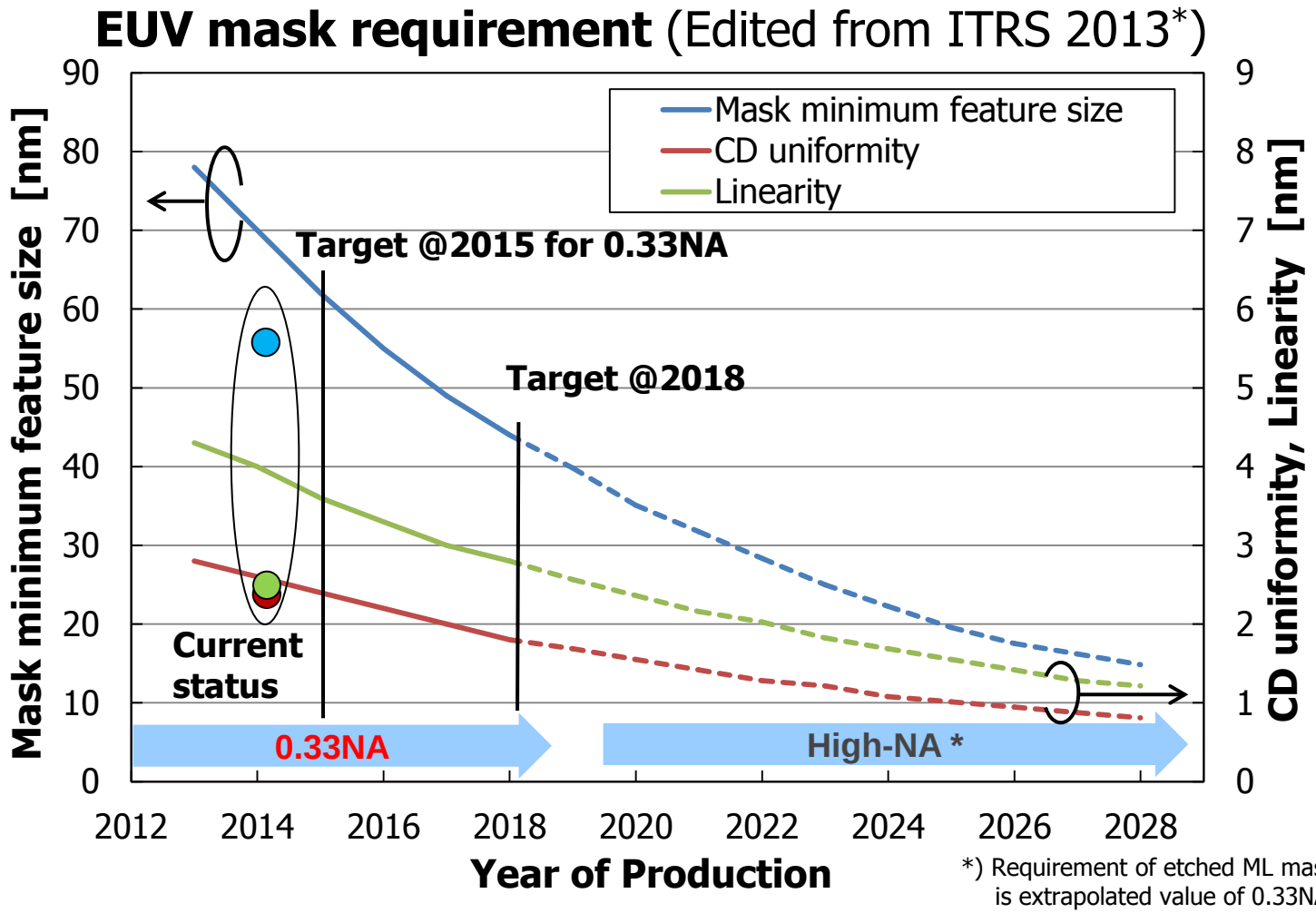
CD Uniformity and Linearity of Etched 20ML Mask



	Target @2015(0.33NA)	Current Capability
CD Uniformity	≤ 2.4 nm	2.4 nm (120mm□)
CD Linearity	≤ 3.6 nm(CD 62nm up)	2.3 nm

Current etched ML mask CD performance catches up EUV mask requirement @2015.

Current Status and Outlook



*) Requirement of etched ML mask for high-NA is extrapolated value of 0.33NA.

Current etched ML mask CD performance catches up EUV mask requirement of 0.33NA @2015.

Continuous improvement is required in order to apply etched ML mask to EUVL production.

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Summary

Defect Management

- ✓ Supply chain management with blank supplier is necessary.
- ✓ Mask handing with dual pod shows encouraging results for the particle requirements of the devices in which redundancy is applicable.
- ✓ Severe particle management is still necessary for EUV mask with pellicle because EUV pellicle proposed by ASML has a gap between mask pattern surface and pellicle frame. New EUV pellicle system attachable only in exposure tool is preferable from the mask fabrication viewpoint.
- ✓ EBEYE M (EB inspection tool) is to be used for particle inspection (~20nm size) in EUV mask handling.

EUVL Extension

- ✓ Etched ML mask is effective in EUVL extension and is ready for 0.33NA exposure.
- ✓ Next Step is to clear the hurdle of defect (inspection and repair).

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